Course Syllabus

VE527

Computer-Aided Design of Integrated Circuits

Summer 2021

Course Description:

The course focuses on the fundamental mathematics, data structures, and algorithms that enable the automatic design of modern very large scale integrated circuits. The content includes: Introduction to computational Boolean algebra such as binary decision diagram and satisfiability; Two-level and multi-level logic synthesis; Technology mapping; Physical design including placement and routing; Timing analysis; Large-scale optimization heuristics such as simulated annealing.

Instructor:

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Office: Room 430, Long Bin Building
Office hour: Monday 7:00 – 8:00 pm and Wednesday 7:00 – 8:00 pm

Textbook (Author, Book Title, Publisher, Publication Year, ISBN):

Laung-Terng Wang, Yao-Wen Chang, and Kwang-Ting Cheng, *Electronic Design Automation: Synthesis, Verification, and Test (Systems on Silicon)*, Morgan Kaufmann, 2009, ISBN 9780123743640.

Course Objectives:

To teach students the fundamental mathematics, data structures, and algorithms for logic synthesis, layout synthesis, verification, and timing analysis.

Course Outcomes:

Get familiar with the fundamental mathematics, data structures, and algorithms for logic synthesis, layout

synthesis, verification, and timing analysis.

Course Prerequisites:

Ve270 Introduction to Logic Design; Ve281 Data Structures and Algorithms.

Course Website:

Log into Canvas at https://umjicanvas.com. Announcements, lecture slides, assignments, and grades will be posted on the class webpage.

Grading Policy (Assignments, Project, Exams, etc.):

There will be 6 written assignments, 2 programming assignments, one midterm exam, and one final exam. The grading distribution is:

Class Participation	4%
Written Assignments	30%
Programming Assignments	16%
Midterm Exam	25%
Final Exam	25%

Any questions about the grading of the assignments or exams must be brought to the attention of the instructor within one week after the item is returned.

Honor Code Policy:

The rules for observing the Honor Code in this course are quite simple: you are allowed to talk about the course work, but you must never show any other student your written work. You are not allowed to write down formulas for another student, let them see your homework (including codes), demonstrate something to them on a blackboard, or use any other type of written communication. Of course, during exams, no communication of any kind (verbal or written) is allowed!

Teaching Schedule: (Subject to Change)

NO.	Date	Lectures and Exams
1	5/10	Course Introduction;

2	5/12	Technology Mapping;
3	5/17	Technology Mapping; Placement: Basics;
4	5/19	Placement: Simulated Annealing Placement;
5	5/24	Placement: Analytical Placement;
6	5/26	Routing: Maze Routing;
7	5/31	Routing: Implementation Details;
8	6/2	Timing Analysis: Basics;
9	6/7	Timing Analysis: Static Timing Analysis;
10	6/9	Timing Analysis: Interconnect Delay Model;
11	6/16	Computational Boolean Algebra: Cofactors and Boolean Difference;
12	6/21	Midterm Exam;
13	6/23	Computational Boolean Algebra: Quantification and Network Repair
14	6/28	Computational Boolean Algebra: Tautology, Positional Cube Notation, and Recursive Tautology Checking
15	6/30	Binary Decision Diagram: Basics
16	7/5	Binary Decision Diagram: Applying Operation and Variable Ordering
17	7/7	Satisfiability: DPLL Algorithm
18	7/12	Satisfiability: Obtain CNF; Two-level Logic Synthesis: Basics
19	7/14	Two-Level Logic Synthesis: Espresso
20	7/19	Multi-Level Logic Synthesis: Algebraic Model and Kernels

21	7/21	Multi-Level Logic Synthesis: Kernels and Extraction
22	7/26	Multi-Level Logic Synthesis: Implicit Don’t Cares
23	7/28	Circuit Partitioning; Floorplanning
24	TBD	Final Exam;