Ve270 Introduction to Logic Design

Summer 2017

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Office Hours: W/Th 10:00am – 12:00pm, or by appointment
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Course Description:
This course is designed to cover binary and non-binary number systems, Boolean algebra, digital design techniques, logic gates, logic minimization, standard combinational circuits, sequential circuits, flip-flops, synthesis of synchronous sequential circuits, programmable logic devices, ROMs, RAMs, arithmetic circuits, and computer-aided design. Laboratory includes design and implementations of digital circuits and systems as well as CAD experiments.

Credits: 4

Prerequisites: Vg101 or equivalent

Course Objectives:
1) To teach the fundamental principles in design and implementation of digital logic circuits including combinational circuits, sequential circuits, and finite state machines.
2) To develop skills in top-down design and bottom-up verification for digital components and systems.
3) To provide hands-on experience with computer aided design tools and programmable logic devices in digital logic design.
4) To improve communication skills to effectively function on a team.

Course Outcomes:
1) Ability to perform simple arithmetic in binary, octal, hexadecimal, BCD number systems
2) Ability to manipulate logic expressions using binary Boolean algebra.
3) Ability to generate the prime implicants of logic functions of 5 or fewer variables using graphical (Karnaugh map) method, and to obtain their minimal two-level implementations with and without don't cares.
4) Ability to analyze and synthesize small multi-level combinational logic circuits containing AND, OR, NOT, NAND, NOR, and XOR gates based on simple delay models.
5) Ability to use basic functional & timing (clocking) properties of latches & flip-flops.
6) Ability to analyze synchronous sequential circuits to extract next-state/output functions
7) Ability to translate a word statement specifying the desired behavior of a simple sequential system into a finite state machine (FSM), to simplify and build the architecture that consists of state register and next state/output logic.

8) An ability to implement simple digital systems using controller and basic datapath components such as registers, memories, counters, multiplexers, ALUs, etc.
9) Basic knowledge of possible issues and restrictions in digital system.
10) Ability to design and test simple digital systems using a hardware description language and CAD tools
11) Knowledge of programmable logic devices and ability of implementing a logic circuit in FPGA.
12) Experience and communication skills to function on a team.

Textbook:

Frank Vahid, *Digital Design 2/e*, John Wiley & Sons, 2010. ISBN 9780470531082

Course Policies:

- **Honor Code:** All students in the class are bound by the Honor Code of the Joint Institute (http://umji.sjtu.edu.cn/academics/academic-integrity/honor-code/). You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.
- Test: The test procedure will be announced prior to the tests. Anyone violating the testing procedure will be given an 'F' for the test.
- Attendance: Attendance will be randomly taken. 5% will be deducted from the final grade for each absence starting from the 4th one.
- Participation: Active participation in course meetings is expected for all students. With each submitted assignment, students should be prepared to explain their solutions to the class.
- Submission: Homework assignments are due on the specified date before the class begins. **No late homework assignments will be accepted**. However, the instructor reserves the right to waive the penalty for emergencies (e.g. hospitalization) or arrangement made with the instructor 24 hours prior to the due date.
- Individual Assignments: Students are encouraged to discuss course topics and homework assignments with each other. However, all submissions must represent your own work. Duplicated submission is not allowed and will trigger an honor code violation investigation.
- Group Assignments: Some assignments will be team efforts. The work submitted must reflect the work of the team. The grade for a group assignment will be shared among the entire team equally, unless specified differently.

Course Outline: *Tentative and subject to change.*

Week	Dates	Topics	Reading
1	5/16	Course introduction, introduction to logic design	1.1 – 1.3, 2.1 – 2.4, 2.8
	5/18	Number systems, basic logic gates, truth table	
2	5/23	Representation of Boolean functions (Lab 1, 1 week)	2.5, 2.6
	5/25	Logic optimization and K-map	6.1, 6.2
3	5/30	**No class** (Lab 2, 2 weeks)	
	6/1	Combinational logic design process and building blocks	2.7, 2.9, 2.10
4	6/6	**No class** (propose to reschedule to 8-9:40am on June 8)	
	6/8	Combinational building blocks	2.7, 2.9, 2.10
	6/8	Latches, Flip-Flops	3.2
5	6/13	Hardware Description Language (Lab 3, 1 week)	9 & Notes
	6/15	Hardware Description Language	

6	6/20	Counters (Lab 4, 1 week)	4.6 – 4.8
	6/22	Registers and shifters	4.1 – 4.5
7	6/27	**Midterm Exam** (Lab 5, 2 week)	
	6/29	FSM and controllers	3.3 – 3.4
8	7/4	FSM and controllers	3.3 – 3.4
	7/6	FSM optimizations and tradeoffs	6.3
9	7/11	FSM optimizations and tradeoffs (Lab 6, 2 weeks)	6.3
	7/13	Arithmetic components	4.9 – 4.10
10	7/18	Arithmetic components	4.9 – 4.10
	7/20	RTL design and examples	5.1 – 5.5
11	7/25	RTL design and examples (Lab 7, 2 weeks)	5.1 – 5.5
	7/27	Timing issues	Lecture Notes
12	8/1	Memory Components	5.7
	8/3	Programmable Logic Devices	Lecture Notes
13	TBD	**Final Exam**	

Course Assessment Methods:

Homework & Quiz:
Homework & quiz problems are designed for students to revisit and synthesize the important concepts in design and analysis of logic circuits they have learned in preceding lectures, and for the instructor to ensure the appropriate delivery and comprehension of important knowledge. Homework & quiz are also assigned for students to gain confidence in engineering problem solving skills on the circuitry, component, and system levels. Typically, one homework set is assigned each week and due in the next week. Students should always be prepared for taking a pop quiz for each homework assignment. In that case, grade of that homework set will be replaced with the grade of the quiz. Two lowest grades for homework/quizzes will be dropped.

Examination:
The examinations shall measure the ability to carry out analysis, design, and verification processes of digital circuits and systems. Examinations are written and paper based. The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis, design, etc.

Lab Experiment:
The labs are designed for students to practice basic understanding of various logic components and logic operations, and to give multiple ways to meet the design requirements. In addition, the labs utilize contemporary software tools in aid of design. Documented design outcomes and/or demonstration of each lab are required following a prescribed format. A team may be randomly quizzed about implementation problems about the labs. Labs will be graded on completeness, correctness, effectiveness in analyzing and presenting lab outcomes.

Special Facilities, Equipments, and Materials Utilized

- Xilinx ISE (sponsored by Xilinx Inc.)
- Xilinx Synthesis Tool (XST, sponsored by Xilinx Inc.)

- Digilent Nexys2 FPGA development boards (partially sponsored by Xilinx Inc.)

Grading Policy:

Homework and Quiz	10%
Lab	30%
Midterm Exam	30%
Final Exam	30%
Total	**100%**

Note: final letter grades will be curved.