



JOINT INSTITUTE
交大密西根学院

Ve311 Electronic Circuits Fall 2018

(Updated on November 13, 2018)

Instructor:

Chang-Ching Tu, Ph.D.

Email: changching.tu@sjtu.edu.cn

Office Hour: Fri 10:00-12:00 at Room 508, JI Building

Teaching Assistant:

Gao Jia

Email: gj_entertain@sjtu.edu.cn

Office Hour: Tue 18:00-20:00 at YLM Center, JI Building

Lecturing:

Mon 14:00 to 15:40 (Middle Hall 412)

Wed 8:00 to 9:40 (Middle Hall 313)

Fri 14:00 to 15:40 (Middle Hall 411)

Labs:

4 labs in total, each with 3 sessions as listed below, at Room 310A (Circuits Lab), JI Building

Mon 8:30 to 12:00

Tue 18:20 to 21:50

Fri 8:30 to 12:00

Homework Assignments:

8 homework assignments in total

Posted on Canvas on Wednesday and due next Wednesday in class

Textbooks:

1. Microelectronic Circuit Design, Richard C. **Jaeger** and Travis N. **Blalock**
2. Design of Analog CMOS Integrated Circuits, Behzad **Razavi**

Course Description:

1. Lecturing: Working principles of nonlinear semiconductor devices, including diode, BJT and MOSFET (with emphasis), and circuits associated with those devices. Particularly, small



signal model, single stage amplifiers, differential amplifiers and current mirrors of MOSFET. Lastly, feedback circuits based on ideal/non-ideal operational amplifiers.

2. Homework Assignment: Circuit analysis by hand-calculation with proper approximations. Comparison of hand-calculation results with Pspice simulation.
3. Lab: Learning how to establish and analyze actual circuits on breadboard by using power supply, function generator, oscilloscope and multimeter.

Course Outcomes:

1. Able to reduce a nonlinear circuit to its small-signal equivalent and analyze it.
2. Able to determine the small-signal model of a transistor from its data sheet and lab measurements using oscilloscopes and function generators.
3. Able to design a digital ring oscillator with a voltage-controllable frequency meeting a given frequency specification.
4. Able to design and physically implement a transistor amplifier having a stable biasing circuit and meeting given design specifications such as gain and node impedances.
5. Able to analyze feedback circuits containing non-ideal operational amplifiers.

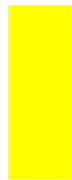
Course Outline:

- Diode
Jaeger and Blalock, page 42 to 95 and 130 to 132
- Diode Circuit
Jaeger and Blalock, page 96 to 129
- BJT
Jaeger and Blalock, page 217 to 255
- BJT Circuit
Jaeger and Blalock, page 786 to 814
- MOSFET
Razavi, page 9 to 46
- MOSFET Single Stage Amplifier
Razavi, page 47 to 99
- MOSFET Differential Amplifier
Razavi, page 100 to 134
- MOSFET Current Mirror
Razavi, page 135 to 165
- Operational Amplifier and Feedback
Jaeger and Blalock, page 544 to 641



Course Schedule:

| | Sep | | | Oct | | | | Nov | | | | Dec | | | | |
|-----------|-----|----|----|-----|----|----|----|-----|----|----|----|-----|----|----|----|----|
| Monday | 10 | 17 | 24 | 1 | 8 | 15 | 22 | 29 | 5 | 12 | 19 | 26 | 3 | 10 | 17 | 24 |
| Tuesday | 11 | 18 | 25 | 2 | 9 | 16 | 23 | 30 | 6 | 13 | 20 | 27 | 4 | 11 | 18 | 25 |
| Wednesday | 12 | 19 | 26 | 3 | 10 | 17 | 24 | 31 | 7 | 14 | 21 | 28 | 5 | 12 | 19 | 26 |
| Thursday | 13 | 20 | 27 | 4 | 11 | 18 | 25 | 1 | 8 | 15 | 22 | 29 | 6 | 13 | 20 | 27 |
| Friday | 14 | 21 | 28 | 5 | 12 | 19 | 26 | 2 | 9 | 16 | 23 | 30 | 7 | 14 | 21 | 28 |
| | 15 | 22 | 29 | 6 | 13 | 20 | 27 | 3 | 10 | 17 | 24 | 1 | 8 | 15 | 22 | 29 |
| | 16 | 23 | 30 | 7 | 14 | 21 | 28 | 4 | 11 | 18 | 25 | 2 | 9 | 16 | 23 | 30 |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | |



Lecturing:

Mon 14:00 to 15:40
Middle Hall 412

Wed 8:00 to 9:40
Middle Hall 313

Fri 14:00 to 15:40
Middle Hall 411



Lab Sessions:

Jl Circuits/Electronics Lab (3F)

Mon 8:30 to 12:00
Tue 18:20 to 21:50
Fri 8:30 to 12:00



Midterm/Final Exam

Instructor Office Hours:

Jl Building Room 508
Fri 10:00 to 12:00

TA Office Hours:

Jl Building YLM Center
Tue 18:00 to 20:00

Grading Policy:

- 8 × Homework Assignments (with Pspice) (16%)
- 4 × Quizzes (4%)
- 1 × Midterm Exam (27%)
- 1 × Final Exam (37%)
- 4 × Lab Reports (16%)

Course Policy:

- Honor Code: All students in the class are bound by the Honor Code of the Joint Institute (<http://umji.sjtu.edu.cn/academics/academic-integrity/honor-code/>). You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.
- Exam: The rule will be announced prior to each exam. Anyone violating the rule will be given an 'F' as the score.



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- Participation: Active participation in course meetings is expected for all students. With each submitted assignment, students should be prepared to explain their solutions to the class.
- Homework Assignments: Students are encouraged to discuss course topics and homework assignments with each other. However, all submissions must represent your own work. Duplicated submission is not allowed and will trigger an honor code violation investigation.