Ve312 Digital Integrated Circuits

Fall 2017

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Course Description:

This course is designed to introduce the MOS technology and other technologies about current integrated circuits designs. Topics like p-n junctions and MOSFETs, the CMOS inverter, combinational logic structures and memories and array structures are discussed during the class. Labs and projects are specially designed to facilitate students to develop skills for software circuit design using Cadance.

Course Objectives:

- Have a brief idea about digital circuit design
- Understand the manufacturing process of CMOS integrated circuits
- Study basic concepts about the diode and the MOS(FET) transistor
- Develop skills for analyzing electrical wire models
- Develop understanding in CMOS inverter

Credits: 4

Course Policies:

• **Honor Code**: All students in the class are bound by the Honor Code of the Joint Institute (see the related sections in JI Student Handbook for details). You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.

• **Quiz**: Quiz will be delivered during the class. Students can discuss problems with others, TAs, instructor or search online, but they should not copy from others.

• **Lab:** Attendance will not be recorded but students should attend the lab to study the skills to use software and finish the tasks delivered by TAs during the lab. Lab report should be finished as part of the assignments.

• **Assignments**: Assignments should be finished on time. If students failed to submit before deadline, they should contact instructor directly to get permissions for late submissions.

• **Project**: Students should form a team of three to finish the final projects. Lab reports are required including specific designs, evaluations about their designs and highlights about the advantages about their designs. The score about the project is based on their delay-energy product.

Course Policies:

Homework*	5%
Midterm Exam	35%
Final Exam	35%
Quiz	5%
Final Project**	20%
Total	100%

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*Individual assignments

**Group assignments