Ve270 Introduction to Logic Design

Summer 2020

Instructor: Gang Zheng, Ph.D.
Office: JI New Building 400E
Contact: (021) 3420-6765 x4005, gzheng@sjtu.edu.cn

Office Hours: Zoom, W 4:00pm – 6:00pm / Th 8:00am – 10:00am, or on Piazza
Classroom: Zoom
Time: T/Th 2:00 – 3:40pm

TA: Mr. ZHAO Wenbo, zhaowenbo@sjtu.edu.cn
Mr. CHEN Yuchi, citrate@sjtu.edu.cn
Ms. TANG Mingyi, tmy19991006@sjtu.edu.cn

Office Hours: TBD

Course Description:
This course is designed to cover binary and non-binary number systems, Boolean algebra, digital design techniques, logic gates, logic minimization, standard combinational circuits, sequential circuits, flip-flops, synthesis of synchronous sequential circuits, programmable logic devices, ROMs, RAMs, arithmetic circuits, and computer-aided design. Laboratory includes design and implementations of digital circuits and systems as well as CAD experiments.

Credits: 4

Prerequisites: Vg101 or equivalent

Course Objectives:
1) To teach the fundamental principles in design and implementation of digital logic circuits including combinational circuits, sequential circuits, and finite state machines.
2) To develop skills in top-down design and bottom-up verification for digital components and systems.
3) To provide hands-on experience with computer aided design tools and programmable logic devices in digital logic design.
4) To improve communication skills to effectively function on a team.

Course Outcomes:
1) Ability to perform simple arithmetic in binary, octal, hexadecimal, BCD number systems
2) Ability to manipulate logic expressions using binary Boolean algebra.
3) Ability to generate the prime implicants of logic functions of 5 or fewer variables using graphical (Karnaugh map) method, and to obtain their minimal two-level implementations with and without don't cares.
4) Ability to analyze and synthesize small multi-level combinational logic circuits containing AND, OR, NOT, NAND, NOR, and XOR gates based on simple delay models.
5) Ability to use basic functional & timing (clocking) properties of latches & flip-flops.
6) Ability to analyze synchronous sequential circuits to extract next-state/output functions

7) Ability to translate a word statement specifying the desired behavior of a simple sequential system into a finite state machine (FSM), to simplify and build the architecture that consists of state register and next state/output logic.
8) An ability to implement simple digital systems using controller and basic datapath components such as registers, memories, counters, multiplexers, ALUs, etc.
9) Basic knowledge of possible issues and restrictions in digital system.
10) Ability to design and test simple digital systems using a hardware description language and CAD tools
11) Knowledge of programmable logic devices and ability of implementing a logic circuit in FPGA.
12) Experience and communication skills to function on a team.

Textbook:

Frank Vahid, *Digital Design 2/e*, John Wiley & Sons, 2010. ISBN 9780470531082

Course Outline: *Tentative and subject to change.*

Week	Dates	Topics	Reading
1	5/12	Course introduction, introduction to logic design	1.1 – 1.3, 2.1 – 2.4, 2.8
	5/14	Number systems, basic logic gates, truth table	
2	5/19	Representation of Boolean functions (Lab 1, 1 week)	2.5, 2.6
	5/21	Logic optimization and K-map	6.1, 6.2
3	5/26	Combinational building blocks (Lab 2, 2 weeks)	2.7, 2.9, 2.10
	5/28	Combinational building blocks	2.7, 2.9, 2.10
4	6/2	Latches, Flip-Flops	3.2
	6/4	Hardware Description Language	9 & Notes
5	6/9	Hardware Description Language (Lab 3, 1 week)	9 & Notes
	6/11	Counters	4.6 – 4.8
6	6/16	Registers and shifters (Lab 4, 1 week)	4.1 – 4.5
	6/18	FSM and controllers	3.3 – 3.4
7	6/23	**Midterm Exam** (Lab 5, 2 weeks)	
	6/25	**No Class (Dragon Boat Festival)**	
8	6/30	FSM and controllers	3.3 – 3.4
	7/2	FSM optimizations and tradeoffs	6.3
9	7/7	FSM optimizations and tradeoffs	6.3
	7/9	RTL design and examples (Lab 6, 2 weeks)	5.1 – 5.5
10	7/14	RTL design and examples	5.1 – 5.5
	7/16	Arithmetic components	4.9 – 4.10
11	7/21	Arithmetic components	4.9 – 4.10
	7/23	Timing issues (Lab 7, 2 weeks)	Lecture Notes
12	7/28	Memory Components	5.7
	7/30	Programmable Logic Devices	Lecture Notes
13		**Final Exam**	

Course Policies:

- **Honor Code:** All students in the class are bound by the Honor Code of the Joint Institute (http://umji.sjtu.edu.cn/academics/academic-integrity/honor-code/) as well as the ***Addendum to the Honor Code for Online Teaching***. You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.
- Test: Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.
- Attendance: Attendance to the lectures is strongly encouraged, not only because difficult concepts are discussed during the lectures, but also because it is an effective way to get engaged in class activities. Attendance to the designated lab sessions is required.
- Participation: Active participation is highly expected for all students. This involves participation in interactive activities during the lecture time, proper assistance to other students in group studying, contributions to the Q&A on Piazza, etc.
- Individual Assignments: Due to the online teaching format, most of the assignments are individual efforts. All submissions must represent your own work. Duplicated submission is not allowed and will trigger an honor code violation investigation. However, students are encouraged to discuss course topics and help each other to understand the problems.
- Group Assignments: Some assignments may be team efforts. The work submitted must reflect the work of the entire team.
- Submission: All assignments should be submitted electronically on Canvas before the specific deadline.

Addendum to the Honor Code for Online Teaching

- The Honor Code in the Context of Online Courses
  The JI Honor Code applies to courses taught in an online fashion in the same way that it does to all courses. It is worth repeating the central tenets here:
  - Engineers must possess personal integrity as students and as professionals. They must honorably ensure safety, health, fairness, and the proper use of available resources in their undertakings.
  - Members of JI are honorable and trustworthy persons.
  - The students, faculty members, and staff members of JI trust each other to uphold the principles of the Honor Code. They are jointly responsible for precautions against violations of its policies.
  - It is dishonorable for students to receive credit for work that is not the result of their own efforts.

  In particular, the parts of the Honor Code regarding conduct during in-class examinations, for coursework, projects etc. apply correspondingly for such work conducted in courses taught online. Additional rules adapted to remote examinations, coursework etc. may be imposed as necessary.

  In addition, students are required to abide by following rules specific to online teaching. These requirements are provisionally considered part of the Honor Code for the current teaching term.

Due to the new types of interaction and the new forms of learning activities there may be further issues that are not covered below. Students should not hesitate to contact their instructor, the Honor Council (jihonor@sjtu.edu.cn) or the FCD (jifcd@sjtu.edu.cn) if they have any questions.

- Online Presence and Activities

  The Joint Institute imposes a "real name" policy for all online activities organized by JI instructors. This policy applies to groups or communication by E-Mail, Canvas, Piazza, Zoom, WeChat and all other platforms where groups are set up by JI or by individual instructors for students attending JI courses, events or other activities.

  Students are required to use their actual name (in Pinyin) as part of their online presence for such groups and when communicating online. Individual instructors may also require students to add their name in Chinese characters (if applicable) and/or their Student ID.

  Unless otherwise noted, such online activities are intended for the exclusive participation of JI students. Account names, meeting IDs, passwords and other information intended to protect the exclusivity of such activities may not be shared with anyone who is not part of the course or activity.

  For example, it is not permissible to give a Zoom meeting ID of a given course to any person who is not enrolled in that course, whether or not the person is a JI student.

- Online Etiquette

  When communicating or otherwise using online groups, students should follow the regulations set down by instructors concerning the use of online tools. Vandalism, spam messages, verbal and other forms of abuse, violation of English-only policies (as detailed by instructors) and disturbance of the learning experience of other students are not permitted.

- Teaching and Learning Materials

  Teaching and learning materials, such as lecture slides, assignments, quizzes, videos etc. are copyrighted and may not be passed on to others without the express permission of the course instructor. This applies in particular to recordings of Zoom lectures and other videos created by instructors.

  In particular, it is not permissible to upload videos to sharing platforms (such as Youku or YouTube) or to post lecture slides, assignment questions, project descriptions etc. on public sites such as SlideShare.

Course Assessment Methods:

Homework & Quiz:
Homework & quiz problems are designed for students to revisit and practice the important concepts in design and analysis of logic circuits they have learned in preceding lectures, and for the instructor to ensure the appropriate delivery and comprehension of important knowledge. Homework & quiz are also assigned for students to gain confidence in engineering problem solving skills on the circuitry, component, and system levels.

Typically, one homework set is assigned each week. However, **submission of homework is NOT required. Instead, students will be given a pop quiz on the due date for each homework assignment**. Two lowest grades for the quizzes will be dropped.

Examination:
The examinations are to measure the level of achievement of the Course Outcomes. Requirements of the examinations will be announced prior to the exams. The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis, design, etc. The exams may be given on paper or online.

Lab Experiment:
The labs are designed for students to practice basic understanding of various logic components and logic operations, and to give multiple ways to meet the design requirements. In addition, the labs utilize contemporary software tools in aid of the design projects.

Due to COVID-19 situation, labs will be take-home individual work until further notice.
Demonstration is required for each lab. Every student will be orally examined about implementation problems in a lab during the demonstration. Labs will be graded on completeness, correctness, effectiveness in analyzing and presenting lab outcomes, oral exam performance, source files, and other required submissions. **No lab grade will be given until all the files are submitted.**

Students should successfully demonstrate a working circuit to the TAs before your lab session ends. **Late demonstration is acceptable with 20% deduction from the lab grade for each day extended until all the points are deducted.**

Grading Policy:

Participation & Etiquette	10%
Weekly Quiz	15%
Lab	40%
Midterm Exam	15%
Final Exam	20%
Total	**100%**

Note: final letter grades will be curved.

Lab grading policy:

Software Simulation and/or Hardware Demonstration	60% of lab grade
Oral Examination	20% of lab grade
Source Files	20% of lab grade

Special Facilities, Equipment, and Materials Utilized

- Xilinx Vivado HLx (WebPACK)
  Download for free at:
  https://www.xilinx.com/member/forms/download/xef.html?filename=Xilinx_Vivado_SDK_2017.2_0616_1_Win64.exe&akdm=0
  (registration needed)
- NI Multisim
  Download the Education Edition evaluation version for free at:
  http://www.ni.com/gate/gb/GB_ACADEMICEVALMULTISIM/US
- Digilent Basys 3 Xilinx Artix-7 FPGA Training board